

CALL FOR GRANT APPLICATIONS

(AE2026-0307)

INESC TEC is now accepting grant applications to award 1 Research Grant (BI) on the scope ODE4ECPIV with reference 101252356 funded by the European Commission under the Horizon Europe program for the period 2021-2027.

1. GRANT DESCRIPTION

Type of grant: Research Grant (BI)

General scientific area: COMPUTER SCIENCE

Scientific subarea: Digital systems, Informatics

Area of Work: Computing, Electronics and Digital Systems

Grant duration: 9 months, starting on 2026-11-11, with the possibility of being renewed for a maximum term of two years, in the cases of students enrolled in a master's degree.

Scientific advisor: João Bispo

Workplace: INESC TEC, Porto, Portugal

Maintenance stipend: € 1090.98, [according to the table of monthly maintenance stipend for FCT grants](#), paid via bank transfer. Grant holders may be awarded potential supplements, according to a quarterly evaluation process (Articles 19, 21 and 22 of the [Regulations for Grants of INESC TEC](#) and Annex II), up to a maximum limit of 50% of the monthly maintenance stipend.

INESC TEC supports costs with registration, enrolment or tuition fees, during the grant duration, under the terms established in the internal document: [Payment of Tuition fees to grant holders](#).

The grant holder will benefit from health insurance, supported by INESC TEC.

2. OBJECTIVES:

To study, develop and evaluate open-source tools and methodologies for the design and integration of heterogeneous digital systems, within the scope of the ODE4EC initiative, with a focus on RISC-V systems and domain-specific accelerators. The work may cover design input from C/C++ code or ONNX models, compilation and hardware synthesis, design space exploration, simulation and co-simulation, verification and workflow automation.

Specific objectives, depending on the area of work:

- To analyse tools and methodologies for design, compilation, simulation and verification, identifying requirements, gaps and opportunities for integration.
- To develop or extend tools to support the design, generation, configuration, integration or verification of processors, accelerators and heterogeneous systems.
- Contribute to hardware/software co-design workflows, design space exploration, simulation, co-simulation, verification and automation.
- Evaluate tools, methodologies or prototypes in representative case studies, assessing functionality, performance,

interoperability and reproducibility.

- Document the results and contribute to their dissemination, including participation in the co-authorship of a scientific article.

3. BRIEF PRESENTATION OF THE WORK PROGRAMME AND TRAINING:

The work plan will focus on one or more of the following areas, depending on the tasks of the project to which the fellowship is allocated:

- Literature review and analysis of relevant tools and workflows, identifying requirements, integration barriers and evaluation criteria.
- Familiarisation with existing tools, architectures and code bases, including system generators, compilers, high-level synthesis (HLS) tools, simulators and electronic design automation (EDA) workflows.
- Development or extension of design input mechanisms, code transformation and generation, compilation, and generation/configuration of RISC-V systems with accelerators, including reconfigurable accelerators such as CGRAs.
- Development and integration of functionality for processors, accelerators, memories and communication interfaces, including, where applicable, custom instructions, numerical formats for artificial intelligence inference and memory-centred computing.
- Development or integration of simulation and co-simulation environments, functional verification, and continuous integration and delivery (CI/CD) workflows, with support for testing and performance analysis.
- Integration and experimental evaluation of prototypes, including exploration of the design space and coordination with synthesis and implementation workflows on FPGAs or ASICs, depending on the selected research area.
- Documentation of the results, drafting of recommendations for ODE4EC and collaboration on the writing of a scientific article and, where applicable, a Master's thesis.

4. REQUIRED PROFILE:

Admission requirements:

Enrollment in a master's degree in Electrical Engineering, Computer Science, or a related field;
The awarding of the fellowship is dependent on the applicants' enrolment in study cycle or non-award courses of Higher Education Institutions.

Preference factors:

- Experience in one or more of the following areas: compilers and code transformation; digital systems design and high-level synthesis (HLS); computer architecture and RISC-V systems; simulation, co-simulation and verification; tool integration, test automation and CI/CD.
- An interest in open-source hardware and tools, heterogeneous systems and hardware/software integration.
- Fluency in Portuguese and English (written and spoken).

Minimum requirements:

- Experience in programming, particularly in C/C++, Python or scripting languages.
- Fluency in English (written and spoken).

5. EVALUATION OF APPLICATIONS AND SELECTION PROCESS:



Selection criteria and corresponding valuation: the first phase comprises the Academic Evaluation (AC), based on the criteria referred to in Article 12 of the [Regulations for Grants of INESC TEC](#), while the second phase comprehends the Individual Interview (EI). All factors are evaluated on a scale of 0 to 100, taking into account the applicants' merit, suitability and conformity with the preference factors.

The weight of the AC factors are as follows: Academic Qualifications (FA, 40%), Scientific Publications (PC, 10%), Experience (EX, 40%) and Motivation Letter (CM, 10%).

Candidates who score less than 50 points in the AC average will be considered excluded on absolute merit. The top five candidates approved on absolute merit will be qualified for the individual interview. The Final Grade (CF) is obtained by the weighted average of AC (70%) and EI (30%).

DISABILITY INCENTIVE

Candidates who present a degree of disability equal to or greater than 90% will benefit from an incentive (20) in the score of the CV Assessment.

Candidates who present a degree of disability equal to or greater than 60% and less than 90% will also benefit from an incentive (10) in the score of the CV Assessment.

Said score may, in these cases, exceed 100 points.

Candidates must demonstrate the degree of disability during the application, namely through the submission of the Multi-Purpose Medical Certificate of Disability, issued in accordance with Decree-Law no. 202/96, of October 23 currently in effect.

Candidates must declare, in the application form, the type of disability used throughout the selection process, in order to proceed with the required adaptations.

The Selection Jury is composed of the following members:

President of the Jury: João Bispo

Full member: Filipe Figueiredo Correia

Full member: Nuno Miguel Paulino

Substitute member: Luis Miguel Pinho

Release of results and prior hearing: the results of the selection process, as well as the terms and procedures for prior hearing, will be released to the applicants by email, under the terms referred to in Article 13 of the Regulations for Studentships and Fellowships of INESC TEC.

6. FORMALISATION OF APPLICATIONS:

Application Documents:

1. Motivation letter;
2. Curriculum Vitae (must include the list of previous fellowships, their type, beginning and end dates, funding entities and host institutions);
3. Certificate or diploma degree;
4. Proof of enrollment in a degree awarding study cycle or in a non degree awarding Higher Education program.
 - The proof of enrollment may be presented just during the grant hiring stage.
5. Signed declaration stating the infringement of the grant holder's duties (article 14, no. 4)
6. Documental evidence to support the country of residence, residence permit or other legally equivalent document, in cases where the applicant is a foreigner or non-resident in Portugal - valid until the beginning of the grant.
7. Other supporting documents relevant to the final assessment.

Failure to deliver the required documents within the 90-day period after the date of the notice of the conditional awarding of the grant implies its cancellation.

Application period: From 2026-10-08 to 2026-10-21

Submission of applications: the application will be formalised by submitting the form available in the *Work With Us* section of INESC TEC website.

7. BINDING LEGISLATION AND REGULATION

The hiring process shall comply with the current legislation regarding the Research Grant Holder Statute, approved by Law no. 40/2004 of August 18, in its current wording, as well as by the [Regulations for Grants of INESC TEC](#) and for [FCT Grants Regulation in force](#).

For more information, please check the [Regulations for Grants of INESC TEC](#) and relevant annexes at www.inesctec.pt/bolsas



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