CALL FOR GRANT APPLICATIONS
(AE2023-0527)

INESC TEC is now accepting grant applications to award 1 Research Initiation Grant (BII) within the scope of the A-MoVeR funded by IAPMEI with reference 45 Co-financed by Component 5 - Capitalization and Business Innovation, integrated in the Resilience Dimension of the Recovery and Resilience Plan within the scope of the Recovery and Resilience Mechanism (MRR) of the European Union (EU), framed in the Next Generation EU, for the period 2021 - 2026.

1. GRANT DESCRIPTION

Type of grant: Research Initiation Grant (BII)

General scientific area: ENGINEERING

Scientific subarea: Electrical engineering

Area of Work: Engineering

Grant duration: 12 months, starting on 2024-02-15.

Scientific advisor: Luís Manuel Pessoa

Workplace: INESC TEC, Porto, Portugal

Maintenance stipend: € 541,12, according to the table of monthly maintenance stipend for FCT grants , paid via bank transfer. Grant holders may be awarded potential supplements, according to a quarterly evaluation process (Articles 19, 21 and 22 of the Regulations for Grants of INESC TEC and Annex II), up to a maximum limit of 50% of the monthly maintenance stipend.

INESC TEC supports costs with registration, enrolment or tuition fees, during the grant duration, under the terms established in the internal document: "Payment of Tuition fees to grant holders".

The grant holder will benefit from health insurance, supported by INESC TEC.

2. OBJECTIVES:

- Enlarge the knowledge of the state of the art regarding the design of printed circuit boards;
- Identification and selection of the most adequate optimization methods to address the proposed workplan:
- Develop the research skills through the application of the selected methods;
- Apply the scientific method on the research process and a critical attitude on the obtained results.

3. BRIEF PRESENTATION OF THE WORK PROGRAMME AND TRAINING:

1. Study MCU architectures from schematic to layout;
2. Design PCB prototype for MCU application;
3. Write code in MCUs;
4. Test and validate a MCU board demonstrator;
5. Write the grand activities report

4. REQUIRED PROFILE:

Admission requirements:

Enrollment in the Licenciatura in Electrical and Computer Engineering.
The awarding of the fellowship is dependent on the applicants' enrolment in study cycle or non-award courses of Higher Education Institutions.

Preference factors:

- Experience in the design of PCBs and MCU programming.

Minimum requirements:

- Experience with electronics simulation tools;
- Experience in electronic experimental setups for circuit test and validation.

5. EVALUATION OF APPLICATIONS AND SELECTION PROCESS:

Selection criteria and corresponding valuation: the first phase comprises the Academic Evaluation (AC), based on the criteria referred to in Article 12 of the Regulations for Grants of INESC TEC, while the second phase comprehends the Individual Interview (EI). All factors are evaluated on a scale of 0 to 100, taking into account the applicants' merit, suitability and conformity with the preference factors.
The weight of the AC factors are as follows: Academic Qualifications (FA, 50%), Scientific Publications (PC, 5%), Experience (EX, 35%) and Motivation Letter (CM, 10%).
Candidates who score less than 50 points in the AC average will be considered excluded on absolute merit. The top five candidates approved on absolute merit will be qualified for the individual interview. The Final Grade (CF) is obtained by the weighted average of AC (70%) and EI (30%).

The Selection Jury is composed of the following members:

President of the Jury: Luís Manuel Pessoa
Full member: Nuno Miguel Paulino
Full member: Joana Santos Tavares
Substitute member:

Release of results and prior hearing: the results of the selection process, as well as the terms and procedures for prior hearing, will be released to the applicants by email, under the terms referred to in Article 13 of the Regulations for Studentships and Fellowships of INESC TEC.

6. FORMALISATION OF APPLICATIONS:

Application Documents:

1. Motivation letter;
2. Curriculum Vitae (must include the list of previous fellowships, their type, beginning and end dates, funding entities and host institutions);
3. Certificate or diploma degree;
4. Proof of enrollment in a degree awarding study cycle or in a non degree awarding Higher Education program.
    - The proof of enrollment may be presented just during the grant hiring stage.
5. Signed declaration stating not having benefited from any other research fellowship (Article 5, no. 5)
6. Documental evidence to support the country of residence, residence permit or other legally equivalent document, in cases where the applicant is a foreigner or non-resident in Portugal - valid until the beginning of the grant.
7. Other supporting documents relevant to the final assessment.

Failure to deliver the required documents within the 90-day period after the date of the notice of the conditional awarding of the grant implies its cancellation.

Application period: From 2023-12-28 to 2024-01-17

Submission of applications: the application will be formalised by submitting the form available in the *Work With Us* section of INESC TEC website.

7. BINDING LEGISLATION AND REGULATION

The hiring process shall comply with the current legislation regarding the Research Grant Holder Statute, approved by Law no. 40/2004 of August 18, in its current wording, as well as by the Regulations for Grants of INESC TEC and for FCT Grants Regulation in force.

For more information, please check the Regulations for Grants of INESC TEC and relevant annexes at www.inesctec.pt/bolsas